Room-temperature single charge sensitivity in carbon nanotube field-effect transistors

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Electrical current fluctuation studies are reported for coaxial *p*-type and *n*-type single-wall carbon nanotube field-effect transistors (FETs). Abrupt discrete switching of the source-drain current is observed at room temperature. The authors attribute these random telegraph signals to charge fluctuating electron traps near the FET conduction channels. Evolution of the current-switching behavior associated with the occupancy of individual electron traps is demonstrated and analyzed statistically. The result strongly indicates room temperature single charge sensitivity in carbon nanotube FETs, which may offer potential applications for single molecule sensors based on suitably prepared FET devices. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2399942]

Carbon nanotubes are potential candidates for nanoelectronic applications such as field-effect transistors and sensors.[1–5] The inherent noise of such devices is important yet few studies have addressed noise issues,[6–9] and these have mainly focused on nanotubes in an "open-to-air" non-passivated configuration. Here we report on electrical current fluctuations in passivated coaxial *p*- and *n*-type single-wall carbon nanotube (SWCNT) field-effect transistors (FETs). Room temperature source-drain current switching between quantized levels is observed in these devices, indicating single charge sensitivity of SWCNT FETs. Our results suggest that suitably designed devices may serve as effective single charged biomolecule detectors at room temperature.

SWCNT FETs were fabricated according to a previously described method.[10–13] Briefly, suspended SWCNTs bridging metal electrodes (Pt/Cr) were grown across gaps etched through freestanding silicon nitride membranes by chemical vapor deposition, and gate dielectrics and gate electrodes were patterned in a coaxial configuration.[11,12] *p*-type FETs were fabricated by coating SWCNTs with a silicon nitride gate dielectric using low-pressure chemical vapor deposition (LPCVD) followed by patterning a metal gate electrode (Au/Cr) on top. Figure 1(a) shows a schematic of a *p*-type FET structure. For *n*-type FETs,[12,13] the SWCNTs are coated with a thermally evaporated layer of Cr (a few nanometer thick), followed by an atomic-layer deposition coating of ~10 nm of Al_2O_3 and a LPCVD coating of silicon nitride (~100 nm).

Figure 1(b) shows the room temperature source-drain current I_{DS} as a function of gate voltage V_g under a source-drain bias $V_{DS}=0.2$ V for a *p*-type SWCNT FET. I_{DS} values were also recorded as a function of time at fixed gate voltages and source-drain bias voltages. Discrete switching of I_{DS} is clearly observed [Fig. 1(c)]. We attribute these random-telegraph signals to charge fluctuating electron traps

near the nanotube channel, as has been observed for narrow-channel complementary metal-oxide semiconductor FETs at low temperatures.[14] Quantized transitions presumably occur when an electron hops from the conducting channel to nearby traps and vice versa, causing the current to switch
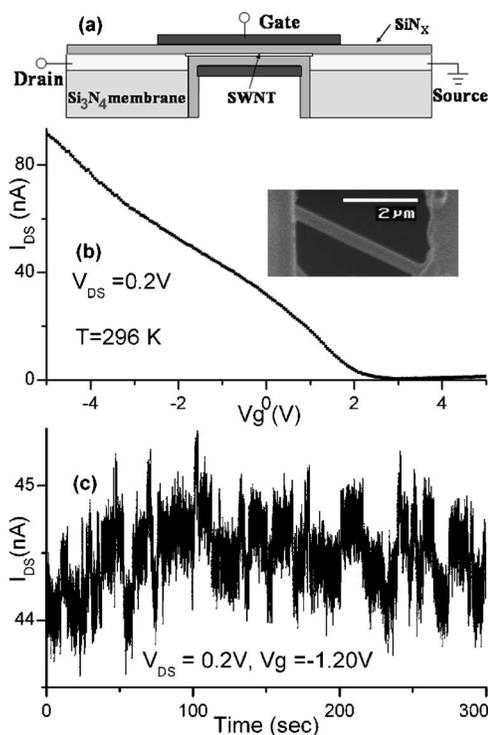

FIG. 1. (a) Schematic of the *p*-type SWCNT FETs. (b) Source-drain current I_{DS} as a function of gate voltage V_g at room temperature for a *p*-type FET made by coating a nanotube with ~150 nm LPCVD silicon nitride in radius as the gate dielectric. Inset: SEM image of the device after the LPCVD coating but before patterning the gate electrode. (c) I_{DS} as a function of time under a source-drain bias $V_{DS}=0.2$ V and gate voltage $V_g=-1.2$ V at room temperature using a sampling rate of 300 Hz and a low-pass filter with a rise-time constant of 3 ms.

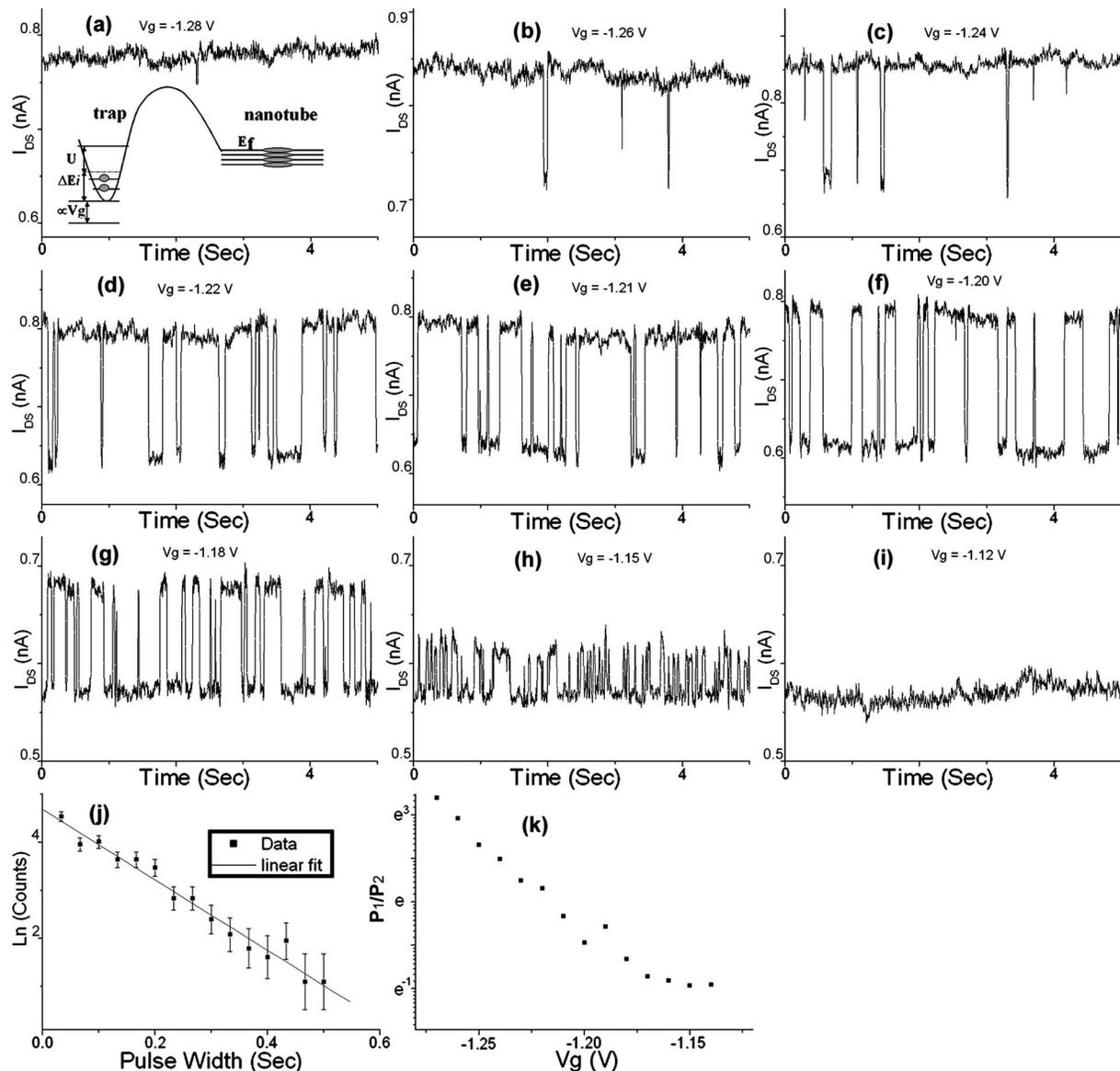[a]Electronic mail: golovchenko@physics.harvard.edu

FIG. 2. [(a)–(i)] Source-drain current I_{DS} as a function of time under fixed source-drain bias $V_{DS}=0.2$ V with different gate voltages at a temperature T =7 K for the sample shown in Fig. 1. (A notch filter of 60 and 120 Hz was utilized.) Inset of (a): Energy diagram of electron tunneling between the nanotube and a nearby electron trap. The energy of the trap state consists of the electrostatic potential induced by V_g, the intrinsic energy spacing ΔE_i, and the Coulomb charging energy U. (j) Statistical distribution of the pulse width of the upper I_{DS} level at $V_g=-1.20$ V. (k) Logarithmic-scale plot of the probability ratio between the upper and the lower level (P_1/P_2) as a function of gate voltage. Data processing in (j) and (k) is based on 100 s recordings of the source-drain current.

between discrete levels. The SWCNT FET contains very few electrons in the conducting channel, so it is not surprising that one can observe switching even at room temperature.

At lower temperatures, it is possible to more clearly resolve and study the two level switching (Fig. 2). At a temperature of $T=7$ K, as V_g sweeps from -1.28 to -1.12 V, the fluctuating current changes from being dominated by an upper level to a state that spends equal times in an upper and a lower level on average, and finally to a state dominated by the lower level [Figs. 2(a)–2(i)]. These observations are explained by a gate-voltage dependent energy shift of an electron trap near the nanotube. As shown in the inset of Fig. 2(a), the energy difference between the trap and the Fermi level of the SWCNT is varied by the change of V_g, modulating the occupancy of the electron trap. An electron hops from the nanotube Fermi level to the trap state as the gate-voltage sweeps towards the positive direction, decreasing the number of effective current-carrying electrons and leading to a lower

source-drain current. (For an ideal quantum ballistic one-dimensional conductor, each current-carrying electron mode gives a conductance of $e^2/h \sim 1/25.8$ kΩ. Hence, it is reasonable that current switching due to the trapping of one electron can be observed. In addition, the Coulomb potential of a charge changing trap may also influence the transmittance of conducting modes in a semiconducting SWCNT.)

Statistically, at a fixed gate voltage, if we assume a constant tunneling rate λ from the conducting channel to the trap, the probability for I_{DS} to switch from the upper to the lower level within times T and $T+\Delta T$ (small ΔT) should be $P=\lambda \Delta T e^{-\lambda T}$. For a small ΔT, ln P should be linearly dependent on T with slope $-\lambda$. Figure 2(j) depicts the distribution of the pulse widths (of the upper level) at $V_g=-1.20$ V based on a 100 s record of I_{DS}. For data analysis, we use ΔT $=1/30$ s. The ordinate represents the logarithmic plot of the number of pulses with a width between t and $t+\Delta T$, where $t=m\Delta T$ is the abscissa (with m being an integer). Linear
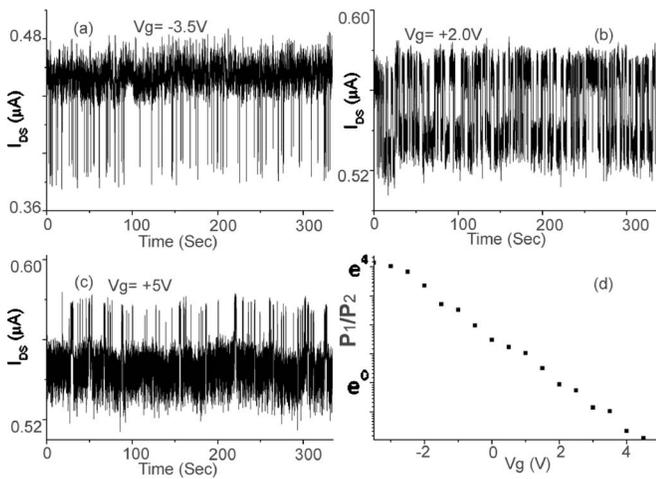
FIG. 3. [(a)–(c)] Source-drain current I_{DS} at room temperature as a function of time under fixed source-drain bias $V_{DS}=-1$ V with different gate voltages for a n-type FET made by coating suspended nanotubes with ∼1.4 nm Cr, and then a combination of 20 nm Al_2O_3 (by atomic-layer deposition) and 100 nm silicon nitride (by LPCVD) in radius as the gate dielectrics. The bottom level in (c) shows fluctuations which may be due to the contribution of another two-state switching on a smaller energy scale. (d) Logarithmic-scale plot of the probability ratio between the upper and the lower level (P_1/P_2) as a function of gate voltage under $V_{DS}=-1$ V for the n-type FET.

fitting gives $\lambda_1=7.3$ 1/s. Since the ratio between the overall duration at the upper level and that at the lower level is near equal at this gate voltage, we expect equivalent tunneling rates: either the electron hops from the SWCNT to the trap, or from the trap to the SWCNT. A similar analysis for the lower level gives nearly identical results as that for the upper level, as expected.

The gate-voltage dependence of the ratio of occupation probabilities for the two levels is obtained by adopting the simple model illustrated in the inset of Fig. 2(a). According to equilibrium statistical mechanics, this probability ratio is given by

$$P_1/P_2 = (g_1/g_2)e^{-\beta(E_f-E_t)} = (g_1/g_2)e^{-\beta\Delta E}, \qquad (1)$$

where g_1 is the degeneracy of the Fermi level, g_2 is the degeneracy of the trap state, E_f is the Fermi energy, and E_t is the trap state energy. (E_t includes contributions of the electrostatic potential induced by V_g, the intrinsic trap energy, and the Coulomb charging energy.)

Assuming a linear dependence of ΔE on V_g, i.e., $\Delta E = ce(V_g - V_0)$, where c and V_0 are constants, $\ln(P_1/P_2)$ should be linearly dependent on V_g. Figure 2(k) shows a plot of $\ln(P_1/P_2)$ as a function of V_g where the ratio of probabilities is taken as the ratio of times spent at the different current levels. A linear dependence holds in most of the transition region of V_g, while increasing contributions from more than one trap can account for the deviation from a linear behavior for $V_g > -1.15$ V.

We also observe current-switching behavior in n-type SWCNT FETs. An evolution of the occupancy of a single-electron trap associated with gate-voltage sweeping is resolved even at room temperature in a n-type coaxial FET (Fig. 3). The discrete random telegraph signals approach ∼20% in relative amplitude at room temperature. The switching strongly suggests single-electron sensitivity at room temperature. Figure 3(d) shows the probability ratio of the two levels as a function V_g, clearly indicating a depen-

dence as predicted by Eq. (1). Linear fitting gives a slope $k = -\beta ec- = -0.79$ 1/V, so our constant $c=0.021$. Using a model of a coaxial cylinder with the gate electrode as the outer equipotential surface and the Cr-coated SWCNT as the inner surface and assuming the SWCNT diameter as ∼2 nm, we estimate the distance of the electron trap to the outer edge of the Cr layer as ∼0.2 nm, placing the trap just outside the nanotube as expected. Taking the degeneracy ratio $g_1/g_2 \sim 1$ in Eq. (1), one can estimate the offset parameter $V_0 \sim 2$ V. At $V_g=0$, this gives an energy difference between the trap state and the nanotube Fermi level as $E_t-E_f \sim 42$ meV.

We note that not all FETs in our experiments show clearly resolvable discrete current switching, but most devices exhibit excess fluctuations without resolvable transitions likely due to the many distributed electron traps. This may be one explanation for the previously observed excess noise in open-air nanotubes.[7] This noise exposes a major challenge to the potential application of carbon nanotubes in electronic devices and it suggests that effort is needed to reliably eliminate traps near the nanotube channel for low noise devices. Electron traps near the interface between the gate dielectrics and the nanotubes contribute most to the random telegraph noise. Optimized gate dielectric processing may enable control of trap distributions in the future.

In summary, we have investigated the electrical current fluctuations of coaxial p- and n-type SWCNT FETs. A discrete random telegraph signal due to the perturbation of electron traps near the conducting channel is clearly indicated. The sensitivity of SWCNTs to a single charge changing event at room temperature may provide opportunities for realizing single biomolecule sensors based on suitably fabricated SWCNT FETs. SWCNT FETs with electron traps may also prove useful for single-spin detection.[15,16]

[1] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature (London) **393**, 49 (1998).
[2] R. Matel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[3] P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, Science **287**, 1801 (2000).
[4] J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai, Science **287**, 622 (2000).
[5] *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications*, edited by M. S. Dresselhaus, G. Dresselhaus, and P. Avouris (Springer, Berlin, 2001).
[6] P. G. Collins, M. S. Fuhrer, and A. Zettl, Appl. Phys. Lett. **76**, 894 (2000).
[7] H. Ouacha, M. Willander, H. Y. Yu, Y. W. Park, M. S. Kabir, S. H. M. Persson, L. B. Kish, and A. Ouacha, Appl. Phys. Lett. **80**, 1055 (2002).
[8] L. Roschier, R. Tarkiainen, M. Ahlskog, M. Paalanen, and P. Hakonen, Appl. Phys. Lett. **78**, 3295 (2001).
[9] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, Nano Lett. **2**, 755 (2002).
[10] H. B. Peng, T. G. Ristroph, G. M. Schurmann, G. M. King, J. Yoon, V. Narayanamurti, and J. A. Golovchenko, Appl. Phys. Lett. **83**, 4238 (2003).
[11] H. B. Peng and J. A. Golovchenko, Appl. Phys. Lett. **84**, 5428 (2004).
[12] H. B. Peng and J. A. Golovchenko, e-print cond-mat/0508670.
[13] Haibing Peng, Ph.D. thesis, Harvard University, 2004.
[14] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, Phys. Rev. Lett. **52**, 228 (1984).
[15] M. Xiao, I. Martin, E. Yablonovitch, and H. W. Jiang, Nature (London) **430**, 435 (2004).
[16] The initial submission of this letter was in August 2005. While the letter was in preparation a related study in low temperature appeared in the literature: F. Liu, M. Bao, H. Kim, K. L. Wang, C. Li, X. Liu, and C. Zhou, Appl. Phys. Lett. **86**, 163102 (2005).